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APPLICANTS:	Irfan Amanat, et al.	§	Confirmation No.: 8199
SERIAL NO.:	09/643,073	§	Group Art Unit: 3624
FILED:	August 21, 2000	§	Examiner: Jagdish Patel
FOR:	Apparatus and Method for Load Balancing Among Data Communications Ports in Automated Securities Trading Systems	§	Atty. Dkt. No.: 1991-01600

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner For Patents
P. O. Box 1450
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Date: February 13, 2006

Sir:

In response to the final office action of June 9, 2005, the appellant files this appeal brief. A notice of appeal was filed via facsimile on November 10, 2005.

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I. REAL PARTY IN INTEREST

The real party in interest is the E*TRADE Financial Corporation, which acquired the assignee Tradescape Technologies LLC by merger.

II. RELATED APPEALS AND INTERFERENCES

Appellant is unaware of any related appeals or interferences.

III. STATUS OF CLAIMS

The status of the claims is as follows:

Originally filed claims:	1-16
Added claims:	17-22
Canceled claims:	none
"Objected to" claims:	10 and 20
Currently rejected claims:	1-9, 11-19, and 21-22
Presently appealed claims:	1-9, 11-19, and 21-22

IV. STATUS OF AMENDMENTS

An amendment is filed concurrently herewith to place claims 10 and 20 in independent form. The claims appendix presumes entry of this amendment.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention is expressed in the instant application as a method and apparatus for load balancing among data communications ports in an automated securities trading system. (1/3) [1]. In accordance with the disclosure, a securities trading system includes a broker-dealer system, a market, and a data communications port between the broker-dealer system and the market. Broker-dealer systems receive orders from customers, send orders to markets, receive responses from markets, and communicate order status to customers. (1/17). Data communications ports are dedicated to particular markets. (1/22). Broker-dealers often add additional ports to their system, so that more than one port is dedicated to a particular market. (2/1).

A problem with data communications ports is that each has limitations upon the number of orders that can be sent through them in a particular period of time or the number of orders without acknowledgments that can be sent through them. (1/22). If more orders arrive than can be sent through a port in a particular period of time, the broker-dealer system is slowed. If a port partially fails or is slowed for mechanical or electrical reasons, the broker-dealer system is also slowed. (1/24). If a port fails completely, the broker-dealer system is disabled with regard to the orders sent to the market served by that port. (1/25).

A first aspect of the invention provides methods of balancing data communications loads among data communications ports in systems for automated trading of securities. (2/15). The method includes sending an electronic message (such as an order) from a broker-dealer system to a market via a port. An acknowledgment of the order is then received through the port. A determination is then made that the port is not overloaded dependent upon at least the electronic

[1] (1/3) refers to the text that begins at page 1, line 3 of Applicant's patent application.

order and the acknowledgment. Of course, for there to be an alternate route to the market, there must be at least two ports connected to the market.[2]

The time between orders and acknowledgments sent through a port is measured. (8/5). It may then be used to calculate various measures of port latency. (8/12). These include instant latency and average latency. (9/3). Alternately, the number of messages sent to the market may be counted, along with the number of acknowledgments. (9/21). A display may then be used to display one or more of these types of latency and/or the number of messages and acknowledgments sent to, and received from, a given market. (8/20) (10/8).

Embodiments of the invention typically function when a new order from a broker-dealer system is available and ready to be sent through a port to a market. (3/11). Prior to sending the new order through the port to the market, it should be determined that the port is a least-loaded port. (13/23). "Least loaded" means that according to some measure of data communications load, the load of the subject port is at least as low as any other port. (14/2). Measures of data communications load useful with the invention include, for example, measure of latency and net order count. (14/5). The latencies in various embodiments are instant latencies, moving average latencies, decaying average latencies, or other forms of latencies. (15/1). In each case, the disclosed embodiments utilize messages and acknowledgments as a basis for calculating the load of a port.

Claim 1 recites:

> A method of balancing data communications loads among data communications ports in systems for automated trading of securities, the systems including at least one broker-dealer system coupled through at least one data communications system to more than one market system, the method comprising:
> sending electronically a first order from a broker-dealer system to a market via a first port connected to said market, there being at least said first port and a second port connected

[2] This language is shorthand for the limitations contained in claims 1 and 11.

between said broker-dealer and said market;
receiving through said first port from said market to which the first port is coupled an acknowledgment of said first order;
sending the acknowledgment from said first port to the broker-dealer system;
determining that the first port is not overloaded, the determination being dependent upon at least the first order, and the acknowledgment; and
sending a second order through the first port to the market, the sending of the second order being dependent upon the determination that the first port is not overloaded.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1) Whether claims 3-9 and 13-19 are properly rejected under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential functional relationships; and

2) Whether claims 1-2, 7, 9, 11-12, 17, 19, 21, and 22 are properly rejected under 35 U.S.C. § 103 as being obvious in view of DeJagger (US Patent 6,473,424).[3]

VII. ARGUMENT

The claims do not stand or fall together. Instead, appellant presents separate arguments for various independent and dependent claims. Each of these arguments is separately argued below and presented with separate headings and sub-headings as required by 37 CFR § 41.37(c)(1)(vii).

A. Rejections Under 35 USC § 112

1. The Rejection of Claims 3-9 and 13-19

In an office action dated June 9, 2005, the Examiner rejected claims 3-5 and 13-19. The Examiner states on page 4, of the Office Action,

[3] The Examiner references a different DeJagger patent at page 4 of the office action dated June 9, 2005, US Patent 6,667,975. Although the '424 and '975 DeJagger patents have largely the same disclosure, the Examiner confirmed in a telephone conversation dated 1/25/06 that the rejection was made under the '424 patent, not the '975 patent.

> Claims 3-9 and 13-19 are rejected under 35 USC 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
>
> Claim 3 recites limitation "net order count for the first port stored in a processor". This limitation does not functionally relate to any process step of the parent claim 1. Claim 3 also is unclear because the limitations "net order count for the first port stored in a processor" and "the net number of orders" lack proper antecedent basis in the claim as claim 1 only refers to a first order and a second order. It is asserted a net order count for the first port must be determined and stored (in a processor) prior to the decrementing step is carried out.
>
> Claim 4 also inherit same defect as its parent claim 3.
>
> Claim 5 recites limitation "an acknowledgment count for the first port stored in a processor". This limitation does not functionally relate to any process step of the parent claim 1. Claim 5 also is unclear because the limitations "an acknowledgment count for the first port stored in a processor" lack proper antecedent basis in the claim as claim 1 only refers to a first order and a second order. It is asserted an acknowledgement count for the first port must be determined and stored (in a processor) prior to the decrementing step is carried out. Claim 6 also inherit same defect as its parent claim 5.
>
> Claim 6 recites limitation "an order count for the first port..exceeds the acknowledgement count for the first port". There is insufficient antecedent basis for this limitation since no step recites determination of an order count for the first port. Claim 1 and 5 only recites the first order and the second order which may be sent through the first port.
>
> Claims 7-9 contain deficiencies similar to claims 4-6. Appropriate corrections are required.
>
> System claims 13-19 corresponds to method claims 3-9 and contain similar deficiencies.

OA of 6/9/05, pp. 2-3.

2. Arguments Relating to Claims 3-4

Claim 3 (and its dependent claim 4) was rejected for inclusion of the term "net order count for the first port stored in a processor" and the limitations "net order count for the first port stored in a processor" and "the net number of orders".

A rejection under 35 USC § 112, second paragraph, is appropriate in only very limited circumstances that are not present in this case.

The Applicants begin by noting that the second paragraph of 35 USC § 112 requires only a reasonable degree of precision when defining the invention of the patent claims. MPEP 2173.02. Some latitude in the manner of expression and the aptness of terms should be permitted even though the claim language is not as precise as the Examiner might desire. *Id.* This goes hand in hand with the well-worn axiom that an applicant can be his own lexicographer, a fundamental principle of the Patent Laws. MPEP 2173.01.

As explained in MPEP 2172.01, a claim does not necessarily fail to comply with 35 USC 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes. *Ex parte Huber*, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965). Applicants wish to direct the Board's attention to the remainder of the second paragraph of MPEP § 2172.01, which emphasizes that absent some clear statement by the applicants, functional interrelationships are not necessary to patentability. *See Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App. 1965) ("[I]t is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result"); *Ex parte Huber*, 148 USPQ 447, 448-49 (Bd. Pat. App. 1965) (A claim does not necessarily fail to comply with 35 USC 112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes)."

The examiner's focus during examination of claims for compliance with the requirement for definiteness of 35 USC 112, second paragraph, is whether the claim meets the threshold requirements of clarity and precision, not whether more suitable language or modes of expression are available. MPEP 2173.02. When the examiner is satisfied that patentable subject matter is

disclosed, and it is apparent to the examiner that the claims are directed to such patentable subject matter, he or she should allow claims which define the patentable subject matter with a reasonable degree of particularity and distinctness. *Id.* (emphasis in original). Only when a claim remains insolubly ambiguous without a discernable meaning after all reasonable attempts at construction must a court declare it indefinite. *Id.*

The Applicants submit to the Board that the inclusion of the "net order count for the first port stored in a processor" does not render the claim insolubly ambiguous and that a rejection of claim 3 under 35 USC § 112, second paragraph, is improper.

Similarly, while the Examiner characterizes the rejection of the limitations "net order count for the first port stored in a processor" and "the net number of orders" for a lack of antecedent basis, the Examiner focuses on the absence of these limitations in claim 1. The Examiner even states that "It is asserted an acknowledgement count for the first port must be determined and stored (in a processor) prior to the decrementing step is carried out."

The basis of the Examiner's rejection is therefore not antecedent basis, but rather claim breadth. The Examiner, however, is not given the right under the Patent Laws to define the metes and bounds of the invention. MPEP 2173.04. The breadth of a claim can be rejected under 35 USC § 112, second paragraph, only where statements from the Applicants outside the application are inconsistent with the disclosed breadth of the invention. *Id.*

For at least these reasons, the indefiniteness rejections of claims 3 and 4 should be reversed.

3. Arguments Relating to Claim 5

Claim 5 recites limitation "an acknowledgment count for the first port stored in a processor". According to the Examiner, this limitation does not functionally relate to any process step of the parent claim 1. As argued above, functional relationships are not required for a claim to be patentable.

Claim 5 also is allegedly unclear because the limitation "an acknowledgment count for the first port stored in a processor" lacks proper antecedent basis in the claim as claim 1 refers only to a first order and a second order. It is asserted an acknowledgement count for the first port must be determined and stored (in a processor) prior to the decrementing step is carried out. Similar to the arguments offered above with respect to claim 1, the Examiner's rejection is merely an attempt to force the Applicants to narrow claim 1. Such an attempt is not proper under 35 USC § 112, second paragraph.

These rejections by the Examiner are misplaced for generally the same reasons as explained above with respect to the functional relationship and antecedent basis rejections of claim 3. The Applicants submit to the Board that the inclusion of the objected to language does not render the claim insolubly ambiguous and that a rejection of claim 5 under 35 USC § 112, second paragraph, is improper. For at least this reason, the indefiniteness rejection of claim 5 should be reversed.

4. Arguments Relating to Claim 6

Claim 6 recites limitation "an order count for the first port...exceeds the acknowledgement count for the first port". The Examiner contends that there is insufficient antecedent basis in claim 6 for this limitation since no step recites determination of an order count for the first port.

The Applicants submit that the Examiner interprets too harshly the requirements of 35 USC § 112, second paragraph. The question is not whether the Applicants have drafted claim 6 in the same manner the Examiner would, but rather whether the claim remains insolubly ambiguous without a discernable meaning after all reasonable attempts at construction. The Applicants submit that claim 6 meets this minimal statutory standard. For at least this reason, the indefiniteness rejection of claim 6 should be reversed.

5. Arguments Relating to Claims 7-9 and 13-19

The examiner contends that claims 7-9 contain deficiencies similar to claims 4-6, and that system claims 13-19 correspond to method claims 3-9 and contain similar deficiencies. For at least the reasons given above, applicants maintain that these claims satisfy the requirements of 35 USC § 112 and accordingly these indefiniteness rejections should be reversed.

B. Rejections Under 35 USC § 103 Over DeJagger

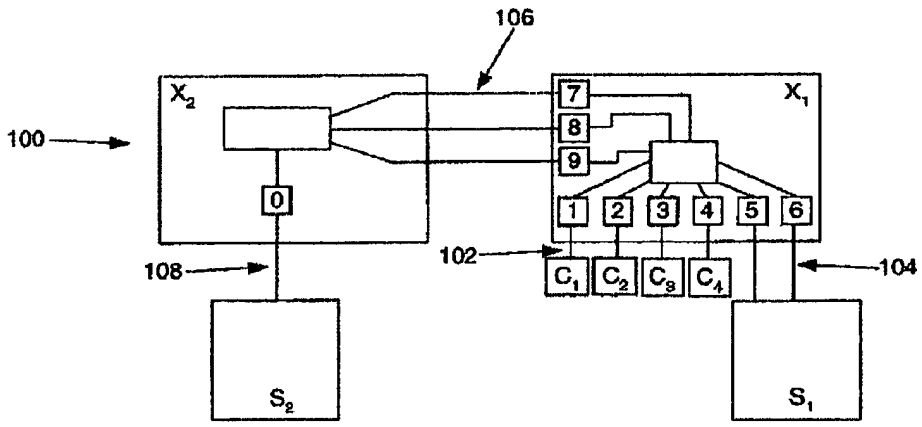
1. DeJagger '424

The Applicant cautions the Board of Appeals that the Examiner mistakenly cited DeJagger US 6,667,975 against the claims at page 4 of the final office action. The Examiner meant to cite DeJagger US 6,473,424. The Examiner confirmed this mistake to the Applicant via a phone conversation on January 25, 2006. Thus, the column and line references made below are to the '424 patent.

The '424 patent is entitled, "Port Aggregation Load Balancing." The system of the '424 patent relates to computer networking.[4] In particular, it relates to balancing the load of data transmissions through a port aggregation.[5]

[4] '424 patent, col. 1, ll. 1-2.

In the excerpted figure below, a common computer network **100** includes a plurality of clients ($C_1 - C_4$), such as personal computers or work stations, connected to each other and one or more servers (S_1, S_2) via a switch (X_1) or router by network cable.[6] Data is forwarded on the network in packets which are typically received by a switch from a source network device and then directed to the appropriate destination device. The receipt and transmission of data packets by a switch occurs via ports (0, 1, 2, 3, 4) on the switch. Packets traveling from the same source to the same destination are defined as members of the same stream.[7]



A bottleneck may be created when several devices are simultaneously attempting to send data to a single other device.[8] One way to relieve this bottle neck is to provide a logical grouping of multiple ports into a single port, sometimes referred to as a port aggregation.[9] Traffic distribution

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[5] *Id.* at col. 2, ll. 47-48.

[6] *Id.* at col. 1, ll. 10-13.

[7] *Id.* at col. 1, ll. 21-27.

[8] *Id.* at col. 1, ll. 31-34.

[9] *Id.* at col. 1, ll. 37-38, 42-43.

for ports grouped in port groups has conventionally been accomplished by static distribution of addresses across the ports of a group.[10]

The '424 patent teaches a method of allocating port assignments based on load, that is the amount of data being forwarded through each port in the group.[11] Packets from a given stream may be forwarded on different ports depending upon each port's current utilization (as defined in the '424 patent).[12]

To help determine the utilization of each port, the '424 patent teaches the use of a pair of time-mark registers and a queue mark indicator.

Because the packets are representative of a stream of data, the packets must not be forwarded out of order. Therefore, the system includes a pair of alternating time-mark registers to assist in determining if any packets of a given stream have been encountered in a given time interval.[13] This information is used in decisions to move a packet stream from one port to another in a port group. To avoid any possibility of packets being received out of order by a downstream device, this mechanism ensures that there has been at least some period of time since the last was forwarded.[14]

The Queue Mark indicator is a way of determining if a transmit queue is current. The transmit queue is a queue of packets to be forwarded on any given port.[15] The transmit queue is

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[10] *Id.* at col. 1, ll. 57-59.

[11] *Id.* at col. 2, ll. 49-52.

[12] *Id.* at col. 2, ll. 54-56.

[13] *Id.* at col. 5, ll. 47-50.

[14] *Id.* at col. 5, ll. 50-55.

[15] *Id.* at col. 4, ll. 65-67.

current when the packets entering the queue (pushed) during a given time interval are the same ones that are exiting the queue (popped).[16] Each time an entry (packet) is pushed onto a transmit queue, the mark bit field of the register is pushed along with it. Each time an entry is popped off a queue (i.e. forwarded), the mark bit field is popped along with it. This popped-off bit value is written to a transmit queue mark indicate register which contains an indication bit for each queue. By comparing the values of the mark bit and the indication bit for a given queue, software can determine, on a queue by queue basis, if that queue is current since the mark bit was last changed. To summarize, a queue is considered current if the indicate bit (that being popped off the queue) equals the mark bit (that being pushed onto the queue) or if the queue is empty.[17]

The dynamic load balancing system of the '424 patent distributes data traffic across the ports in a group based on transmit queue depth.[18] The steps in which the time mark and queue mark indicators are used for dynamic load balancing is explained in the '424 patent by reference to Figure 3B. These steps are not detailed in this Appeal Brief because the exact sequence of steps is not important for the purposes of this appeal.

2. Rejection of Claims 1 and 11

In the final office action dated June 9, 2005, the Examiner rejected claim 1. The Examiner states on page 4, of the Office Action,

> As per claim 1, DeJagger teaches a method of balancing data communications loads among data communications ports in systems (see abstract). DeJagger teaches sending data from a computer system (clients C1, C2 etc. in Figure 1) to a server (server S1 in Figure 1) via a first port wherein there is at least first port and a second port connected between the computer system and the server (ports 1, 2, 3

[16] *Id.* at col. 6, ll. 21-24.

[17] *Id.* at col. 7, ll. 3-5.

[18] *Id.* at col. 63-65.

> etc. Figure 1), receiving through said first port from the server to which the first port is coupled an acknowledgment of data packet, and sending the acknowledgement from the first port to the server (these step is inherent because as disclosed at col. 2 L 49-55 which states that the "load balancing ..is ..dynamic, that is, packs from a given stream may be forwarded on different ports depending each port's current utilization), determining that the first port is not overloaded, the determination being dependent upon at least the data (see col. 2 L 66- col. 3 L 5, "determining whether a prior packet having that stream ID has been distributed to a queue on a port in the group during a predetermined time interval."), and sending a second data packet through the first port to the server, the sending of the order being dependent upon the determination that the first port is not over loaded (see col. 2 L 66-col. 3 L5 distribution of traffic over ports where multiple packets are data are being transmitted. As discussed herein the data packets are allocated to the first port and the second port depending upon the load condition and thus the determination of overload of data traffic and subsequent sending a second data packet through the first node based upon the determination that the first port is not overloaded is inherently indicated. Col. 6 L 24-28, "packets being received ..downstream device.." which inherently teaches presence of a data packet and acknowledgment of the receipt of the data packet by a down stream device).

OA of 6/9/06, pp. 4-5.

As already noted, although the office action references the '975 DeJagger patent, the Examiner confirmed to the Applicant that he meant to cite the DeJagger '424 patent.

The rejection of claim 11 was made on identical grounds.

3. Arguments Regarding Claims 1-2 and 7, 9, 11-12, 17, 19, 21 and 22

Independent claim 1 recites "receiving through said first port from said market to which the first port is coupled an acknowledgment of said first order". Independent claim 11 recites a similar limitation. Claims 2, 7, 9, 12, 17, 19, 21 and 22 depend from these independent claims.

The Examiner asserts that this limitation is inherently disclosed by DeJagger at 2:49-55, which states, "load balancing ... is ... dynamic, that is, packets from a given stream may be forwarded on different ports depending on each port's current utilization." It is notable that despite express explanation in the '424 patent of how dynamic load balancing is carried out in the '424

patent, the Examiner makes no reference to these details. As explained above, the dynamic load balancing system of the '424 patent utilizes a queue mark indicator showing whether the transmit queue for a port is current. *See* DeJagger 5:2-5 and 7:20-57. The transmit queue, in turn, is current when the packets entering the queue (pushed) during a given time interval are the same ones that are exiting the queue (popped). This is tracked by a set of registers. The '424 patent makes no mention, and does not rely upon, whether there has been an acknowledgment received to a message (order).

In order for a teaching to be inherent in a reference, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference. It may not be established by probabilities or possibilities. *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999). Given this standard for inherency, the requirement of an acknowledgment is clearly *not* inherent in DeJagger because dynamic load balancing can be achieved in ways that do not necessitate receiving message (order) acknowledgments. For example, the '424 patent explains from columns 5 to 9 a manner in which dynamic load balancing can be accomplished without the use of an acknowledgment.

For at least this reason, independent claims 1 and 11 (along with their dependent claims 2, 7, 9, 12, 17, 19, 21 and 22) are allowable over the '424 patent.

C. Conclusion

For the reasons stated above, appellants respectfully submit that the rejections should be reversed for the reasons given above. Applicants believe that they have complied with each requirement of the appeal brief. If any member of the Board of Appeals has any questions or

otherwise feels it would be advantageous, he is encouraged to telephone the undersigned at (713) 238-8055.

In the course of the foregoing discussions, appellant may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims.

It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 CFR § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Conley Rose, P.C. Deposit Account Number 03-2769/1991-01600/HDJK.

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VIII. CLAIMS APPENDIX

This listing of claims is the current version of the pending claims in the application.

1. (Previously presented) A method of balancing data communications loads among data communications ports in systems for automated trading of securities, the systems including at least one broker-dealer system coupled through at least one data communications system to more than one market system, the method comprising:

sending electronically a first order from a broker-dealer system to a market via a first port connected to said market, there being at least said first port and a second port connected between said broker-dealer and said market;

receiving through said first port from said market to which the first port is coupled an acknowledgment of said first order;

sending the acknowledgment from said first port to the broker-dealer system;

determining that the first port is not overloaded, the determination being dependent upon at least the first order, and the acknowledgment; and

sending a second order through the first port to the market, the sending of the second order being dependent upon the determination that the first port is not overloaded.

2. (Previously presented) The method of claim 1 wherein determining that the first port is not overloaded comprises:

determining that a latency for the first port is less than a maximum allowed latency for the first port, wherein latency comprises a measure of the speed with which markets return acknowledgments for orders.

3. (Previously presented) The method of claim 1 further comprising:

decrementing a net order count for the first port stored in a processor, wherein the net order count indicates a net number of orders sent through the first port to the market for which acknowledgments have not yet been received from the market, wherein the net order count is decremented after receiving a new acknowledgment.

4. (Previously presented) The method of claim 3 further comprising the steps of:

determining that the net order count for the first port is less than a maximum allowed net order count for the first port, wherein the maximum allowed net order count indicates the maximum number of orders without acknowledgments allowed to be sent through the first port, wherein the net order count being less than the maximum allowed net order count for the first port indicates that the first port is not overloaded; and

incrementing the net order count after receiving a new order.

5. (Previously presented) The method of claim 1 further comprising:

incrementing an acknowledgment count for the first port stored in a processor, wherein the acknowledgment count represents the number of acknowledgments received through the first port during a defined period of time.

6. (Previously presented) The method of claim 5 further comprising the steps of:

determining that an order count for the first port exceeds the acknowledgment count for the first port by at least a maximum allowed net order count, wherein the order count represents the number of orders sent through the first port during the defined period of time, wherein the maximum allowed net order count indicates the maximum number of orders without acknowledgments allowed to be sent through the first port, wherein the order count for the port exceeding the acknowledgment count for the port by at least a maximum allowed net order count indicates that the port is not overloaded; and

incrementing the order count for the first port.

7. (Previously presented) The method of claim 1 further comprising determining, before sending the second order through the first port to the market, that the first port is a least-loaded port, wherein sending the order through the first port to the market is dependent upon determining that the first port is a least-loaded port.

8. (Previously presented) The method of claim 7 further comprising:

determining a net order count for said first port, wherein the net order count for the first port

indicates the net number of orders sent through the first port to the market for which acknowledgments have not yet been received from the market, and any other ports coupled to the market also having net order counts, wherein determining that the first port is a least-loaded port comprises determining that the net order count for the first port is not greater than any of the net order counts for the other ports coupled to the market.

9. (Previously presented) The method of claim 7 further comprising:

determining latency for said first port, wherein said latency comprises a measure of the speed with which markets return acknowledgments for orders, wherein any other ports coupled to the market also have latencies, wherein determining that the first port is a least-loaded port comprises determining that the latency for the first port is not greater than any of the latencies for the other ports coupled to the market.

10. (Previously presented) A method of balancing data communications loads among data communications ports in systems for automated trading of securities, the systems including at least one broker-dealer system coupled through at least one data communications system to more than one market system, the method comprising:

sending electronically a first order from a broker-dealer system to a market via a first port connected to said market, there being at least said first port and a second port connected between said broker-dealer and said market;

receiving through said first port from said market to which the first port is coupled an acknowledgment of said first order;

sending the acknowledgment from said first port to the broker-dealer system;

determining that the first port is not overloaded, the determination being dependent upon at least the first order, and the acknowledgment; and

sending a second order through the first port to the market, the sending of the second order being dependent upon the determination that the first port is not overloaded;

determining, before sending the second order through the first port to the market, that the first port is a least-loaded port, wherein sending the order through the first port to the market is dependent upon determining that the first port is a least-loaded port;

determining a net order count and a latency for said first port,

wherein the net order count for said first port indicates the net number of orders sent through the first port to the market for which acknowledgments have not yet been received from the market,

wherein latency for the first port comprises a measure of the speed with which markets return acknowledgments for orders, wherein any other ports coupled to the market have corresponding net order counts and latencies, wherein determining that the first port is a least-loaded port comprises determining that the product of the net order count for the first port multiplied by the latency for the first port is not greater than the product of the net order count and the latency for any of said other ports coupled to the market.

11. (Previously presented) A load balancing system for automated trading of securities in which data communications loads are balanced among data communications ports, the load balancing system coupled to a multiplicity of ports organized so that one market is coupled to the broker-dealer system through more than one port, the load balancing system operative when a new order from a broker-dealer system is available and ready to be sent through a port to said market, the load balancing system operative continually in turn upon each port assigned to said market, the load balancing system comprising:

computer memory;

at least one computer processor coupled for data communications to said computer memory and said broker-dealer system, and coupled through said data communications ports to more than one market, the processor programmed to:

receive through a port from a market to which the port is coupled an acknowledgment of a first order;

send the acknowledgment to the broker-dealer system;

determine that the port is not overloaded, the determination being dependent at least upon the first order, and the acknowledgment, and

send a second order through the port to the market, the sending of the second order being dependent upon the determination that the port is not overloaded; and

store in said computer memory by the processor the acknowledgment and the second order.

12. (Previously presented) The load balancing system of claim 11 wherein the processor programmed to determine that the port is not overloaded determines that a latency for the port is less than a maximum allowed latency for the port, wherein latency comprises a measure of the speed with which markets return acknowledgments for orders.

13. (Previously presented) The load balancing system of claim 11 further comprising the processor being programmed to decrement a net order count for the port, wherein the net order count indicates the net number of orders sent through the port to the market for which acknowledgments have not yet been received from the market, wherein the net order count is decremented in response to receiving a new acknowledgment.

14. (Previously presented) The load balancing system of claim 13 further comprising the processor being programmed to:

determine that the net order count for the port is less than a maximum allowed net order count for the port, wherein the maximum allowed net order count for the port indicates the maximum number of orders allowed to be sent through the port without corresponding acknowledgments, wherein the net order count being less than the maximum allowed net order count for the port indicates that the port is not overloaded; and

increment the net order count upon an order being sent through said port after said determination that the net order count for the port is less than the maximum allowed net order count for the port.

15. (Previously presented) The load balancing system of claim 11 further comprising the processor being programmed to increment an acknowledgment count for the port, wherein the acknowledgment count represents the number of acknowledgments received through the port during a defined period of time.

16. (Previously presented) The load balancing system of claim 15 further comprising the processor being programmed to:

determine that an order count for the port exceeds the acknowledgment count for the port by at

least a maximum allowed net order count, wherein the order count represents the number of orders sent through the port during the defined period of time, wherein the maximum allowed net order count indicates the maximum number of orders without acknowledgments allowed to be sent through the port, wherein the order count for the port exceeding the acknowledgment count for the port by at least a maximum allowed net order count indicates that the port is not overloaded; and

increment the order count for the port.

17. (Previously presented) The load balancing system of claim 11 further comprising the processor programmed to determine, before sending the second order through the port to the market, that the port is a least-loaded port, wherein sending the second order through the port to the market is dependent upon the determination that the port is a least-loaded port.

18. (Previously presented) The load balancing system of claim 17 wherein a data structure for the port maintained in one of said processors comprises a net order count for the port, wherein the net order count indicates the net number of orders sent through the port to the market for which acknowledgments have not yet been received from the market, and other ports coupled to the market also have data structures maintained in said processors and having net order counts, wherein the processor programmed to determine that the port is a least-loaded port also is programmed to determine that the net order count for the port is not greater than any of the net order counts for the other ports coupled to the market.

19. (Previously presented) The load balancing system of claim 17 wherein a data structure for the port maintained in one of said processors comprises latency, wherein latency comprises a measure of the speed with which markets return acknowledgments for orders, wherein the other ports coupled to the market have data structures having latencies, wherein the processor programmed to determine that the port is a least-loaded port also is programmed to determine that the latency for the port is not greater than any of the latencies for any other ports coupled to the market.

20. (Previously presented) A load balancing system for automated trading of securities in which

data communications loads are balanced among data communications ports, the load balancing system coupled to a multiplicity of ports organized so that one market is coupled to the broker-dealer system through more than one port, the load balancing system operative when a new order from a broker-dealer system is available and ready to be sent through a port to said market, the load balancing system operative continually in turn upon each port assigned to said market, the load balancing system comprising:

computer memory;

at least one computer processor coupled for data communications to said computer memory and said broker-dealer system, and coupled through said data communications ports to more than one market, the processor programmed to:

receive through a port from a market to which the port is coupled an acknowledgment of a first order;

send the acknowledgment to the broker-dealer system;

determine that the port is not overloaded, the determination being dependent at least upon the first order, and the acknowledgment, and

send a second order through the port to the market, the sending of the second order being dependent upon the determination that the port is not overloaded; and

store in said computer memory by the processor the acknowledgment and the second order.

determine, before sending the second order through the port to the market, that the port is a least-loaded port, wherein sending the second order through the port to the market is dependent upon the determination that the port is a least-loaded port;

wherein a data structure for the port maintained in said processors comprises a net order count and a latency, wherein the net order count indicates the net number of orders sent through the port to the market for which acknowledgments have not yet been received from the market, wherein latency comprises a measure of the speed with which markets return acknowledgments for orders, wherein any other ports coupled to the market have data structures comprising net order counts and latencies, wherein the processor programmed to determine that the port is a least-loaded port also is programmed to determine that the product of the net order count for the port multiplied by the latency for the port is not greater than the product of net order

count and latency for any other port coupled to the market.

21. (Previously presented) The method of claim 1, said determination being made upon at least the presence of the first order, and the presence of the acknowledgment.

22. (Previously presented) The system of claim 11, wherein determining that the port is not overloaded is dependent at least upon the presence of the first order, and the presence of the acknowledgment.

IX. EVIDENCE APPENDIX

Not Applicable.

X. RELATED PROCEEDINGS APPENDIX

Not Applicable.